accepting a voltage from a power supply input to the integrated circuit;

accepting a pad voltage from an external voltage source;

comparing the power supply voltage to a predetermined value; and

coupling the pad voltage to a bias for the integrated circuit when the power supply is below the predetermined value.

2. A method as in claim 1 wherein the generation of the bias voltage comprises:

coupling the pad voltage into a drain of a PMOS (P-channel Metal Oxide Semiconductor) device; and

coupling the power supply voltage into a gate of the PMOS device.

3. (Amended) A method as in claim 2 wherein using the pad voltage to generate a bias voltage for the integrated circuit further comprises using the source voltage of the PMOS device to couple the pad voltage to the bias voltage.

4. (Amended) A method as in claim 2 wherein coupling the pad voltage into the drain of a PMOS (P-channel Metal Oxide Semiconductor) device comprises:

providing the pad voltage to an input of a plurality of diode connected MOS devices; and

coupling an output of the plurality of diode connected MOS devices to the drain of the PMOS device.

5. (Amended) A method for generating a bias voltage (bias_mid) from a pad voltage (Vpad), when a power supply (V_{DDO}) is not present the method comprising:

providing V_{DDO} to a control electrode of a first semiconductor device;